GAU/2814

AMENDMENT TRANSMITTAL LETTER

Docket No. M4065.0067/P067

Application No.	Filing Date	Examiner	Group Art Unit
09/118,080	July 17, 1998	A. Chambliss	2814

Applicant(s): Warren M. Farnworth

Invention: LEAD OVER CHIP SEMICONDUCTOR DEVICES WITH A BALL GRID ARRAY (AS AMENDED)

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	19	- 20 =		x	
Independent Claims	4	- 3 =		x	
Multiple Dependent Claims (check if applicable)	☐				
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00

☒ Large Entity ☐ Small Entity

☒ No additional fee is required for this amendment.

☐ Please charge Deposit Account No. _____ in the amount of $ _____. A duplicate copy of this sheet is enclosed.

☐ A check in the amount of $ _____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 04-1073 as described below. A duplicate copy of this sheet is enclosed.

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☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Dated: November 14, 2001

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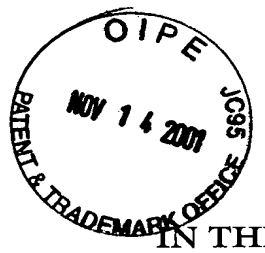


Docket No.: M4065.0067/P067
(PATENT)

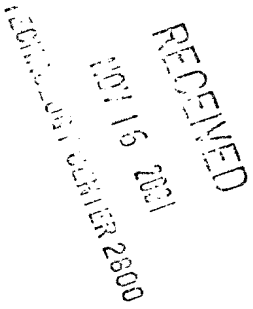
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Warren M. Farnworth

Application No.: 09/118,080 Group Art Unit: 2814

Filed: July 17, 1998 Examiner: A. Chambliss

For: LEAD OVER CHIP SEMICONDUCTOR DEVICES WITH A BALL GRID ARRAY



AMENDMENT

Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the Office Action dated August 14, 2001 (Paper No.14), please amend the above-identified U.S. Patent application as follows:

IN THE CLAIMS:

Rewrite claims 1, 10 and 13 as follows:

C1

1. (Three Times Amended) A semiconductor device, comprising:
a semiconductor chip;
a single dielectric layer;
electrically conductive leads on said dielectric layer; and

C1

a low temperature curing adhesive material that cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit, said low temperature curing adhesive material being located between said semiconductor chip and said dielectric layer.

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10. (Three Times Amended) A taped semiconductor product, comprising:

integrated circuits formed in semiconductor material;

C2

a tape having openings aligned with said integrated circuits, wherein said tape includes a single dielectric layer and electrically conductive leads, said leads being printed on said single dielectric layer;

bond wires extending through said openings, said bond wires being electrically connected to said integrated circuits; and

adhesive material between said tape and said integrated circuits, wherein said adhesive material cures to about ninety percent of its maximum strength within twenty four to thirty six hours at room temperature.

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13. (Three Times Amended) A tape for manufacturing semiconductor devices, said tape comprising:

a single dielectric layer having openings;

C3

electrically conductive leads associated with said openings, said leads being printed on said dielectric layer; and

a low temperature curing adhesive material that cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit, said low temperature curing adhesive material being located between said semiconductor chip and said dielectric layer.

REMARKS

Claims 1, 10 and 13 have been amended. Claims 1-7 and 10-33 remain in the application[1]. Claims 19-30 are withdrawn from consideration. Reconsideration is respectfully requested in view of the claims as amended.

The present invention is directed at the use of a printed tape to form leads on chip ("LOC") semiconductor devices with ball grid arrays ("BGA"). As shown in Figs. 1-2, a semiconductor wafer 10 containing a plurality of semiconductor chips 14 is almost entirely covered by a tape 12. Each chip contains integrated circuits, which are not separately shown on the diagrams. The tape 12 comprises an adhesive layer 20, a single dielectric layer 22, and leads 24, 26, 28, 30. The adhesive layer 20 may be formed of a low temperature, steadily curing material. Preferably, the adhesive material cures to ninety percent of its maximum strength within twenty four to thirty six hours at about room temperature (about seventy five degrees Fahrenheit), and to ninety percent of its maximum strength within two to three hours at about one hundred fifty degrees Fahrenheit. The adhesive layer ideally exhibits low curing shrinkage and reduced stress on the wafer surface 32. See page 8, lines 1-8.

In contrast, Schrock is directed to a method of attaching a bumped semiconductor dice to substrates such as printed circuit boards utilizing an *instant* curing adhesive 34 formulated to cure to about 90 -100% of its maximum strength within 0.25 to 60 seconds (col. 4, lines 56-65). The method includes the steps of heating the die 10 and aligning the contact bumps 12 on the die 10 to the contacts 12 on the substrate 30. Next, the die 10 is brought into contact with the substrate 30, having adhesive material dispensed thereon, to form an adhesive layer 34. Hence, the adhesive layer 34 is almost immediately cured by the heated die 10 rather than steadily curing it, as in the present invention.

[1] The Office Action incorrectly states that claim 9 is pending. Claim 9 was canceled in the Amendment filed January 12, 2001.

Further, in Schrock, the adhesive layer 34 is not actually heated. Rather, the die 10 is heated first and then placed in contact with the adhesive layer 34 to instantly cure it. However, in the present invention, the adhesive layer 20 itself is steadily cured after the tape 12 is placed on the wafer 10.

Claims 1-7, 10-18 and 31-33 are rejected under 35 U.S.C. § 103 as being unpatentable over Heo and Schrock (U. S. Patent No. 6,221,691) in view of Khandros. Reconsideration is respectfully requested. Claim 1, as amended, relates to a semiconductor device that has, among other things, an adhesive material located between a semiconductor chip and a dielectric layer. As recited in claim 1, as amended, the adhesive material cures "to about ninety percent of its maximum strength within two to three hours." This is an important feature of the claimed invention. As explained above for example, in page 8 of Applicant's specification, the low temperature, steadily curing adhesive material exhibits low curing shrinkage and reduced stress on the wafer surface 32. Schrock fails to disclose or suggest the adhesive material of amended claim 1. Heo and Khandros are cited for other features. Accordingly, the rejection of claim 1 should be withdrawn. Claims 2-7 depend from claim 1 and should be allowable along with claim 1 and for other reasons.

Claim 10 relates to a taped semiconductor product with adhesive material between the tape and the integrated circuits, where the adhesive material cures to about ninety percent of its maximum strength within twenty four to thirty six hours at about room temperature. Neither Schrock, Heo nor Khandros teach or suggest this important aspect of the claimed invention. As discussed above, Schrock utilizes an *instant* curing adhesive 34 formulated to cure to about 90 -100% of its maximum strength within 0.25 to 60 seconds. Accordingly, claim 10, and dependent claims 11 and 12, should be considered allowable.

Claims 13-18, as amended, similarly to amended claim 1, each recite "adhesive material that cures to about ninety percent of its maximum strength within two to three hours." Schrock, Heo and Khandros, even when considered in combination, fail to

disclose or suggest this important feature of the claimed invention. Accordingly, the rejection of claims 13-18 should be withdrawn.

Claims 31-33 are rejected under 35 U.S.C. § 103 as being unpatentable over Heo in view of Khandros and Tsukagoshi. Reconsideration is respectfully requested. The Office Action does not provide any motivation for combining the teachings of Heo with that of Khandros nor Tsukagoshi. Note, in order for an obviousness rejection to be proper, there must be a convincing line of reasoning to support the Examiner's rejection. See, Ex parte Clapp, 227 U.S.P.Q. 972, 973 (Bd. App. 1985). The prior art must have suggested to those of ordinary skill in the art they should make the claimed invention. In re Vaeck, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991). Further, the suggestion to combine references must be found in the prior art and not in the Applicants' disclosure. Id. There is no such suggestion for the claimed invention evident in the teachings of the references.

Claims 31-33 recite an "anisotropically conductive adhesive material" located between the dielectric layer 82 and the semiconductor chip 76. The Office Action provides no explanation, as to why the anisotropically conductive adhesive taught by Tsukagoshi should be used in place of the adhesive means 30 of Heo. The conductive property of the Tsukagoshi material would serve no purpose in the Heo product. In other words, there is no suggestion to combine these references. The rejection of claims 31-33 amounts to nothing more than an improper hindsight attempt to reconstruct the claimed invention by picking and choosing isolated features from prior art references without any reason suggested for combining the features together. The rejection of claims 31-33 should be withdrawn. Allowance of the application is solicited.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: November 14, 2001

Respectfully submitted,

By _____

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